

# ATENT BSTRACTS OF APAN

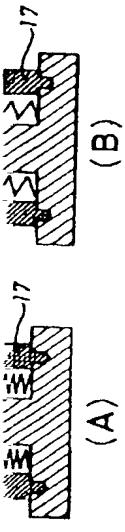
UNEXAMINED  
APPLICATIONS

February 5, 1993

 FIELD

THE PATENT OFFICE  
JAPANESE GOVERNMENT

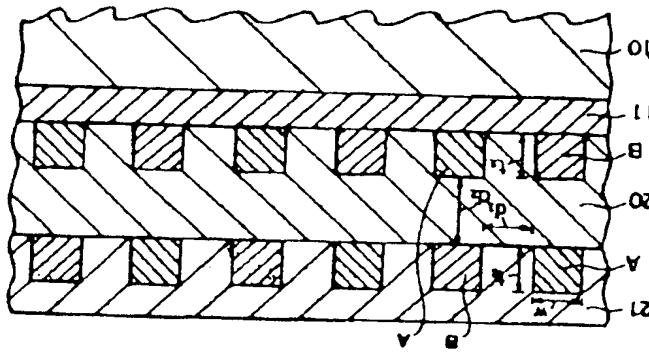
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(54) CAPACITOR OF INTEGRATED CIRCUIT  
 (11) 4-268756 (A) (43) 24.9.1992 (19) JP  
 (21) Appl. No. 3,29961 (22) 25.2.1991  
 (71) MITSUBISHI ELECTRIC CORP (72) HARUFUSA KONDO(1)  
 (51) Int. Cl<sup>5</sup> H01L27/04

**PURPOSE:** To enable a capacitor to be enhanced in capacitance by a method wherein one of a pair of opposed electrodes confronts the other electrode through the intermediary of a dielectric in an upper wiring layer, a lower wiring layer, and between the upper and the lower wiring layer.

**CONSTITUTION:** A lower wiring layer 20 and an upper wiring layer 21 are formed on a board 10 through the intermediary of an interlayer insulating film 11. In the lower wiring layer 20 and the upper wiring layer 21, the electrodes A and B are so arranged as to enable their comb-toothed parts to be engaged with each other. Furthermore, in the upper wiring layer 21, the comb-toothed parts of the electrodes are arranged in AB, AB order, and in the lower wiring layer 20, the comb-toothed parts of the electrodes are arranged in BA, BA order. Therefore, the electrode A of the lower wiring layer 20 confronts the electrode B of the lower wiring layer 21, and the electrode B of the lower wiring layer 21 confronts the electrode A of the lower wiring layer 20. Charge is stored in these three planes, so that a capacitor of this design can be enhanced in electrode area.



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(54) MANUFACTURE OF SEMICONDUCTOR DEVICE  
 (11) 4-268757 (A) (43) 24.9.1992 (19) JP  
 (21) Appl. No. 3-50756 (22) 23.2.1991  
 (71) SONY CORP (72) MAMORU SHINOHARA  
 (51) Int. Cl<sup>5</sup> H01L27/04,H01L27/108